Temperature controller for diode lasers Rev. 3

M. Prevedelli
mrp@fci.unibo.it

November 18, 2009

Introduction

We would like to design a temperature controller for diode lasers good enough for high performance applications but also fairly versatile to be happily used in less critical applications. First of all we should specify the design requirements:

1) The temperature sensors are standard 10kΩ at 25C° thermistors.
2) The operating range of the controller should be $10C^\circ$ for precision applications and $20C^\circ$ for less demanding cases. Experience shows that ranges of $15-25C^\circ$ or $10-30C^\circ$ are usually adequate.
3) The sensor resolution should be at least 1mK. The error introduced by a ±5C° room temperature variation should be below 1mK. Accuracy is not critical.
4) The output circuit should be capable of a maximum current of ±3A for driving high power peltier (i.e. for MOPAs). The circuit should also be easy to modify for higher currents.
5) The error processor is a standard PI(D) controller.
6) The circuit should run from a single polarity supply.
7) It should be easily adapted to a voltage–controlled current source for coils etc.

Thermistors

Usually linear outputs for the measured temperature Tmeas and the set point Tset are desirable. Thermistors however are nonlinear devices. If a digital error processor is used it is easy to compute Tmeas from the thermistor resistance

$R(T)$. With an analog PID the linearization must be implemented in hardware. Note that very high linearity is usually not needed.

The standard thermistor equation is

$$R(T) = R(T_0) \exp\left(\frac{\beta}{T} - \frac{\beta}{T_0}\right) \tag{1}$$

Where T_0, T and β are measured in K, T_0 is the reference temperature (usually 298K i.e. $25C^\circ$) and $R(T_0)$ is the nominal resistance at T_0. The value specified for β by BetaTherm (`http://www.betatherm.com`) for its 10kΩ components is $3892K$. Keep in mind that the tolerance for the best series is of the order of 0.1% from the theoretical curve.

We have that the resistance at $15C^\circ$ is 15.4kΩ, at $20C^\circ$ is 12.4kΩ, and at $25C^\circ$ is, of course, 10kΩ. If we place $R(T)$ in series with a fixed resistor of value $R = R(T_0)$ and expand the division ratio ρ of the voltage divider when $T = T_0 + \Delta T$ with $\Delta T \ll T_0$ we obtain, up to the third order in $\Delta T/T_0$,

$$\rho = \frac{1}{2} \pm \frac{\alpha}{4}\frac{\Delta T}{T_0} \mp \frac{\alpha}{4}\left(\frac{\Delta T}{T_0}\right)^2 \mp \frac{\alpha(\alpha^2 - 12)}{48}\left(\frac{\Delta T}{T_0}\right)^3 \tag{2}$$

with $\alpha = \beta/T_0 \simeq 13$ at room temperature. The sign of the linear term in ΔT depends on the position of the thermistor in the divider (+ when the thermistor is above). The ratio between the second and first order is simply $\Delta T/T_0$. Since in our case $|\Delta T|$ is no more than $5K$ and $T_0 = 293K$ while $\alpha \sim 13$, the second and third order terms introduce a maximum nonlinearity of the order of 1.7% and 0.4% respectively.

For better linearity the value of the fixed resistor can be adjusted. If $\gamma = R/R(T_0)$ then the choice $\gamma = (\alpha - 2)/(\alpha + 2)$ cancels the second order term. The expansion for ρ can then be written as

$$\rho = \frac{1}{2} \pm \frac{1}{\alpha} \mp \left(\frac{\alpha}{4} - \frac{1}{\alpha}\right)\frac{\Delta T}{T_0} \pm \frac{\alpha(\alpha^2 - 4)}{48}\left(\frac{\Delta T}{T_0}\right)^3 \tag{3}$$

The resistor required in our case will be around 9.1 kΩ

The sensitivity should be of the order of

$$\frac{d\rho}{dT} = \frac{\beta}{4T_0^2} \sim 0.0113/C^\circ \tag{4}$$

In Fig 1. is plotted the output of a voltage divider formed by a 10kΩ thermistor in series with a 12.4kΩ driven by a $\pm$ 1.235V voltage obtained from a bandgap reference and a precision inverter. A linear fit in the 20 ± 5 C° range has a slope of 27.9 mV/C° and a maximum error of about 1%. Reducing the resistor to 9.1kΩ improves linearity as expected but moves the 0V output at $27.2C^\circ$. The bridge should then be driven by +1.235V and -1.683V requiring an amplifier with a precise gain of 1.326. A complication that we will happily avoid.

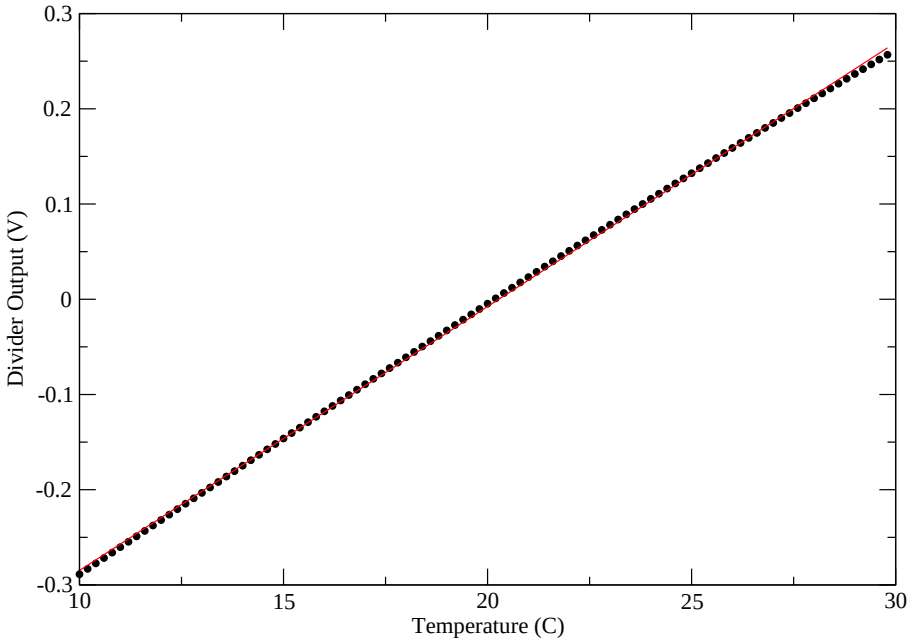

Figure 1: Output of a linearized thermistor. See text for details.

Schematics

The complete schematics is shown in Figs. 2–4. We start from the voltage reference VR1 (a Linear Technology LT1004–1.2), a 1.235±0.004V reference with a thermal coefficient of 20 ppm/C°. VR1 requires a bias current of only 100μA according to the datasheet however run it at at least 1 mA.. The -1.235V are generated using IC3, an AMP03, used as a precision inverter. Since the gain resistors are inside the chip and have been laser trimmed both the accuracy of the initial value and thermal drift should be excellent.

The two voltages drive a divider formed by the thermistor (not visible in the schematics) and by R2, a stable (15 ppm/C°) 0.1% 12.4kΩ resistor. The current in the thermistor is of the order of only 100 μA so self–heating should be negligible.

The response of divider is, as seen above, around 27.9 mV/C°. The signal is buffered and amplified by IC1, an OP177, with a gain of 9 for a response of 250 mV/C°.

The thermal coefficient of V_m, the output of IC1, should be better than 200 ppm/C° to meet our design goal of a variation of less than 1 mK for 5C° of change in the temperature of the external environment.

The thermal coefficient of V_m is influenced by several factors. First of all there is the stability of the gain of IC1, fixed by the ratio of R3 and R4. Their thermal coefficient is 15 ppm/C° and their ratio should be even more stable

since they are at the same temperature.

The voltage divider has a coefficient of about 28 mV/C° so the offset voltage drift of IC1 should be less than 5.6μV/C°. The OP177 is specified for 0.1 μV/C°. The bias current of IC1 should also vary by no more than 1 nA/C° (i.e. 6 μV on the impedance given by the parallel of R2 and R_T. Typical values for the OP177 are below 20 pA/C°. The output of the voltage divider V_d is given by

$$V_d = \frac{(V_r - GV_r)R2}{R2 + R_T} + GV_r \tag{5}$$

where V_r is the VR1 output voltage and G is the gain of IC3. The sensitivities of V_d to V_r, G and R2 changes can be readily evaluated as

$$\frac{\partial V_d}{\partial V_r} = \frac{(1-G)R2}{R2+R_T} + G \simeq \frac{R2 - R_T}{R2 + R_T} \tag{6}$$

$$\frac{\partial V_d}{\partial G} = \frac{-V_r R2}{R2+R_T} + V_r \simeq 0.5V_r \tag{7}$$

$$\frac{\partial V_d}{\partial R2} = V_r(1-G)\frac{R_T}{(R2+R_T)^2} \simeq \frac{V_r}{2R2} \tag{8}$$

$$\tag{9}$$

where we have let $G \simeq -1$ and $R2 \simeq R_T$.

The sensitivity to V_r changes (20 ppm/C°) is attenuated by at least a factor 10 in the $15-25C^\circ$ reaching about 2.5μV/C° at the extremes of the temperature range.

The gain drift with temperature for IC3 is about 2 ppm/C° causing a drift of 1.2μV/C° in V_d.

Finally since the drift of R2 is 15 ppm/C°, it produces a V_d drift of about 9μV/C°. The thermal drift on R2 is then the main source of error and misses the design specs by about a factor 1.5. Better resistors are available (i.e. vishay MPR24 series) with temperature coefficients of 5 ppm/C° but except when the highest stability is required it is probably not worth bothering.

To summarize, the sensitivity of the measured temperature vs. the circuit temperature is of the order of 320 μK/K (or 1mK every 3K), dominated by the thermal coefficient of R2.

Since the output of IC1 swings by $\pm$1.25V in our temperature range we can connect a 20kΩ set point pot. (JP1) directly between $\pm V_r$. In this way the pot. is used ratiometrically so its thermal coefficient cancels and staying below 200 ppm/C° should not present any problem (use a good 10 turns wirewound pot. anyway). The pot. is buffered by IC2 to generate the set voltage V_s. If you do not have at hand the OP177 an AD711 or similar decent precision op. amp. can still be adequate for IC1 and IC2. Use however the same model for both of them in order to have similar output impedances. The error signal V_e is generated by IC4, an AMP03. The common mode signal at the input of IC4 can be as high as 1.2V so the CMRR required to introduce an error of less than

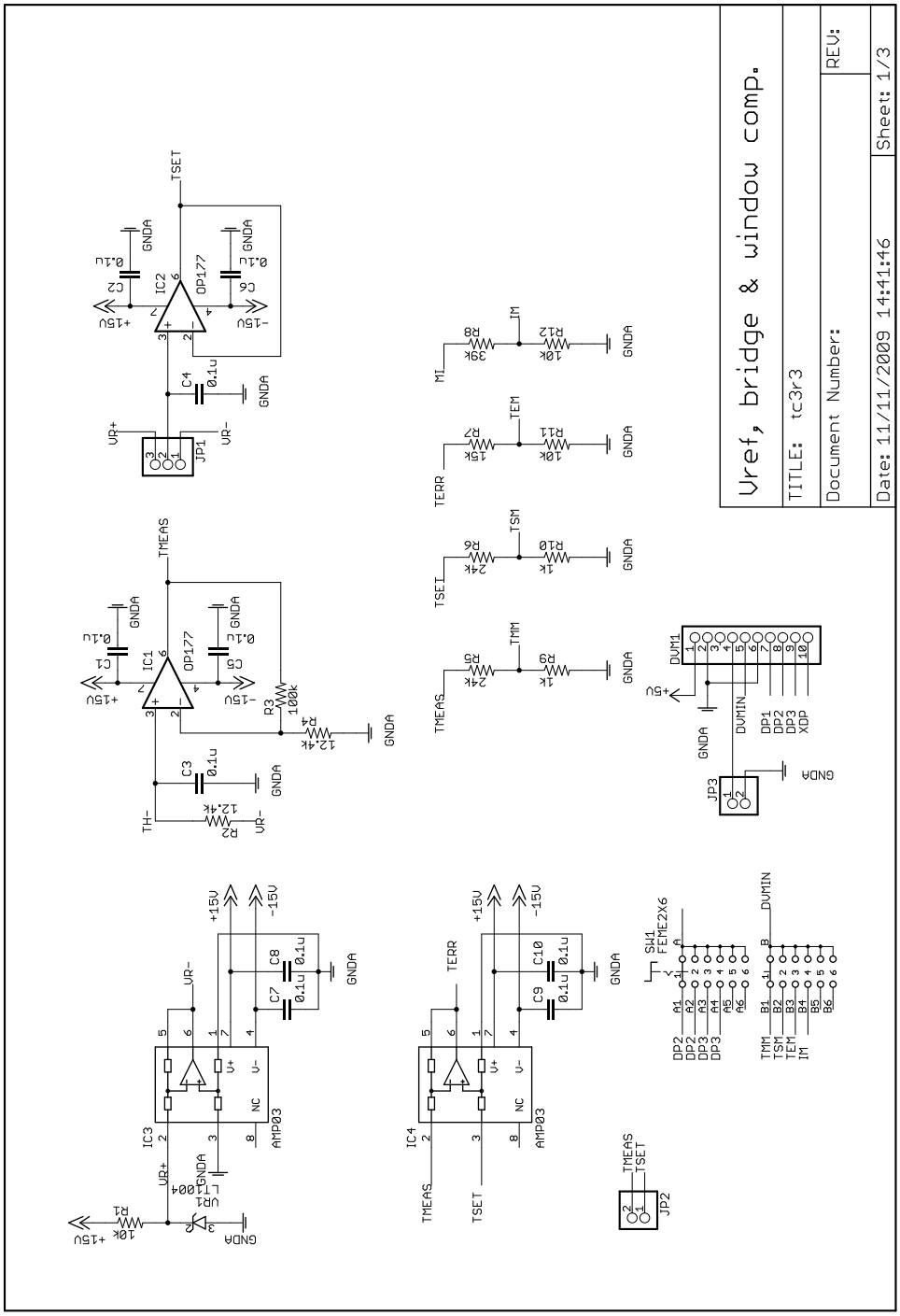

Figure 2: Voltage reference, measured and set temperature, error signal.

1mK is about 74 dB. Since the output impedances of IC1 and IC2 are matched and low this should not be a problem.

The three outputs V_m, V_s and V_e are rescaled by the voltage dividers formed by the six resistors R5–R7, R9–R11 to 10 mV/K for V_m and V_s and to 100 mV/K for V_r. The divider formed by R8 and R12 scales the Peltier current (see Fig. 4) to 100 mV/A.

The four dividers feed the dual selector 4 to 1 SW1 which provides the input for a ±200.0mV LCD DVM connected to DVM1. Wiring is for a Lascar DPM1AS–BL model. Use JP3 to turn on back–illumination.

Note that 0V will correspond to $20C^\circ$ for V_m and V_s and that the current will be only positive. If you do not want an LCD but just a BNC to connect an external DVM and change the voltage dividers as needed. Keep a series resistor in any case if possible.

In Fig. 3 are shown the schematics of the error processor. The PID controller is IC5B. It is an integrator with two additional poles and a zero. The integration time is set by C15 and a T network formed by R15,R16,R19 and R20. With the values indicated in the schematics the integration time can be varied from 10s to 100s. Usually 10s to 20s is a typical integration time for a Hänsch type laser diode cavity. The equivalent resistance of the T network can be as high a 50MΩ so use a low–leakage capacitor for C15 (i.e. not two back–to–back 4.7μF tantalum capacitors) and C13.

The first zero is set by C15 and R21 and is the crossover between integral and proportional action. A second zero (crossover between proportional and derivative action) can be implemented using C13 to bypass the integration resistance. Finally the resistor R13 stops the derivative behaviour at R13 C12.

The reason for the two zeros are the poles introduced by the thermistor time constant (about 1s) and the phase shift due to the delay introduced by the distance between the Peltier and the thermistor. Again experience shows that this zero, for Hänsch type cavities is at few seconds. If possible place R21, R13 and C12 on sockets and adjust as required. It is not a good idea to replace R21 with a trimmer on the front panel. Use JP7 if you need to short C15 during calibration (i.e. with Ziegler–Nichols method or similar).

The integrator drift should be compared with $50\mu\mathrm{V}/C^\circ$ for the requested stability. The drift of the offet voltage of IC5 is clearly not a problem. In the worst (100s integration time) case the drift of I_b should be below 1 pA/C°. The typical value for the AD713 is about 4 pA/C°, adequate below 20s of integration time or so. Find a better op. amp. for long integration times. Be aware that due to the absence of a guard ring in the PCB the circuit is not suited anyway for very long integration times. The integrator is reset using a SPDT switch connected to JP5 to drive two electronic switches in IC7 (IC7A, IC7D), a DG413 or equivalent. IC7B is used to turn on a LED1 when the integrator is on.

The adjustable voltage divider formed by R14 and R18 can be used as a current limiter. The voltage at its output is converted to a current via R35 (see Fig. 4). With the values in this schematic the maximum current is around 5A at most. Adjust R18 for different values.

IC5A, IC6 and the surrounding components are an absolute value circuit

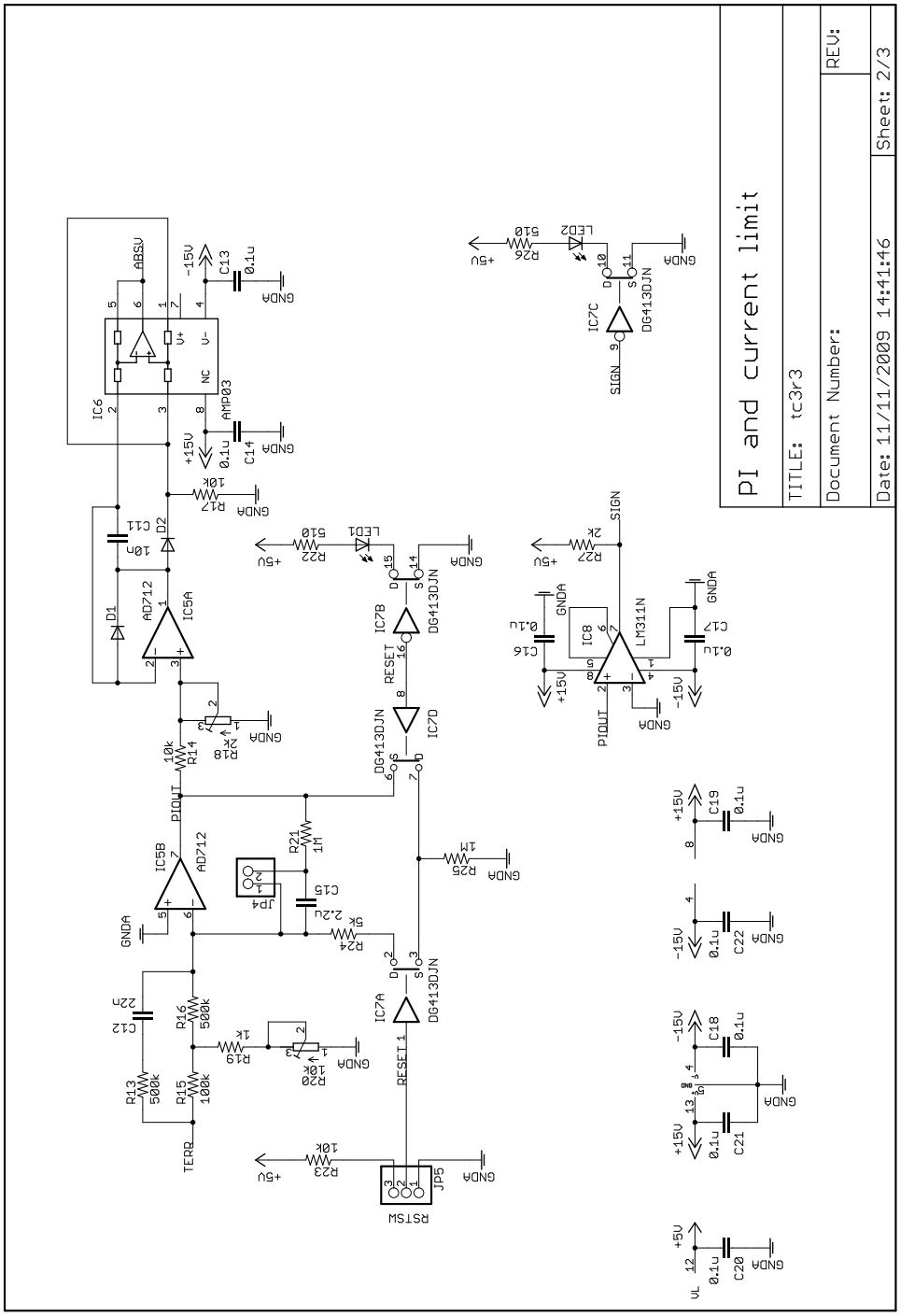

Figure 3: Error processor.

copied from a Burr–Brown application note. IC6 is used as a precision $G = -1$ amplifer. Is totally wasted in a temperature controller but is required if a precision Voltage–Controlled Current Source (VCCS) is required.

IC8 reads the sign of the servo signal. The sign of the servo signal is also monitored by LED2 indicating the cooling/heating status. Again, for a temperature controller IC8 does not need to accurate or stable but if a VCCS is required use an improved LM311 compatible, like the LT1101.

The absolute value and sign signals are used to drive the H–bridge shown in Fig. 4. The bridge is formed by Q1–4, four enhancement type N channel MOSFETs (IRF1010). Only two of them are connected at a time: either Q1 and Q4 or Q2 and Q3. Q3 and Q4 act as switches while Q1 or Q2 form a constant current source with IC11 (any single supply rail–to–rail input op. amp. i.e. a AD820). The current sensing resistor is R35. The MOSFET gates are driven by four SPST switches in IC9. The bridge allows cooling and heating effectively reversing the Peltier connection when the servo signal changes sign. R28, R29 and C31 can be used to reduce the bandwidth of IC9. Too much bandwidth can lead to oscillations due to the gate capacitance of Q1–2. Be careful when implementing a VCCS.

The bridge can be powered from the +5V supply or from a dedicated supply connected to pin 18 and 26 of the 15 poles rear DIN connector. Use JP5 and JP6 to select. Q1–4 and R35 are connected to a simple heat sink even if in normal conditions Q1, Q2 and R35 are dissipating very little power.

The 5V used by the DVM and the logic part of IC7 and IC9 are generated by IC10. In this way the 5V supply is not required if using a dedicated supply for the load. R30 pins the ground of the bridge supply close to the ±15V ground.

The maximum compliance of the bridge is limited to about 10V by the maximum gate voltage of Q1–2 i.e. 15V.

Part List

The silkcreen of the circuit is shown in Fig. 5. Here is the part list:

Qty	Value	Parts	Notes
6	10kΩ	R1,R11–12,R14,R17, R23	
2	12.4kΩ	R2,R4	1/8W, 0.1%, 15ppm C°
1	100kΩ	R3	1/8W, 0.1%, 15ppm C°
2	24kΩ	R5–6	
1	15kΩ	R7	
1	39kΩ	R8	
3	1kΩ	R9–10,R19	
2	500kΩ	R13,R16	
5	100kΩ	R15,R31–34	
2	1MΩ	R21,R25	

Qty	Value	Parts	Notes
2	510Ω	R22,R26	
1	5kΩ	R24	
2	2kΩ	R27–28	
1	200Ω	R29	
1	100Ω	R30	
1	0.5Ω	R35	TO220 package
1	2kΩ	R18	10 turns trimmer
1	10kΩ	R20	10 turns trimmer
1	20kΩ	JP1	10 turns w.w. pot.
2	vk200	L1–2	
26	0.1μF	C1–10,C13–14,C16–24 C26,C28–31	
1	10nF	C11	
1	22nF	C12	
1	2.2μF	C15	Plastic film
2	22μF	C25,C27	
2	1N4148	D1–2	
2	LED	LED1–2	
4	IRFIZ34	Q1–4	
1	LT1004	VR1	1.2V ref. 20 ppm/C°
2	OP177	IC1–2	Precision Op. Amp.
3	AMP03	IC3–4,IC6	Differential Amp.
1	AD712	IC5	Dual FET Op. Amp.
2	DG413	IC7–9	Quad. SPST switch
1	LM311	IC8	LT1011 for VCCS
1	78L05	IC10	+5V, TO92
1	AD820	IC11	Single Supply RR Op. Amp.
1	SW1	SW1	FEME PCB 2x6
1	DPM1AS–BL	DVM1	±200mV Lascar LCD DVM
1	SPDT	JP5	Reset switch
1	H15ML	X1	15 pins DIN41612
1		X2	9 pins Sub D
1		JP8	Monitor output

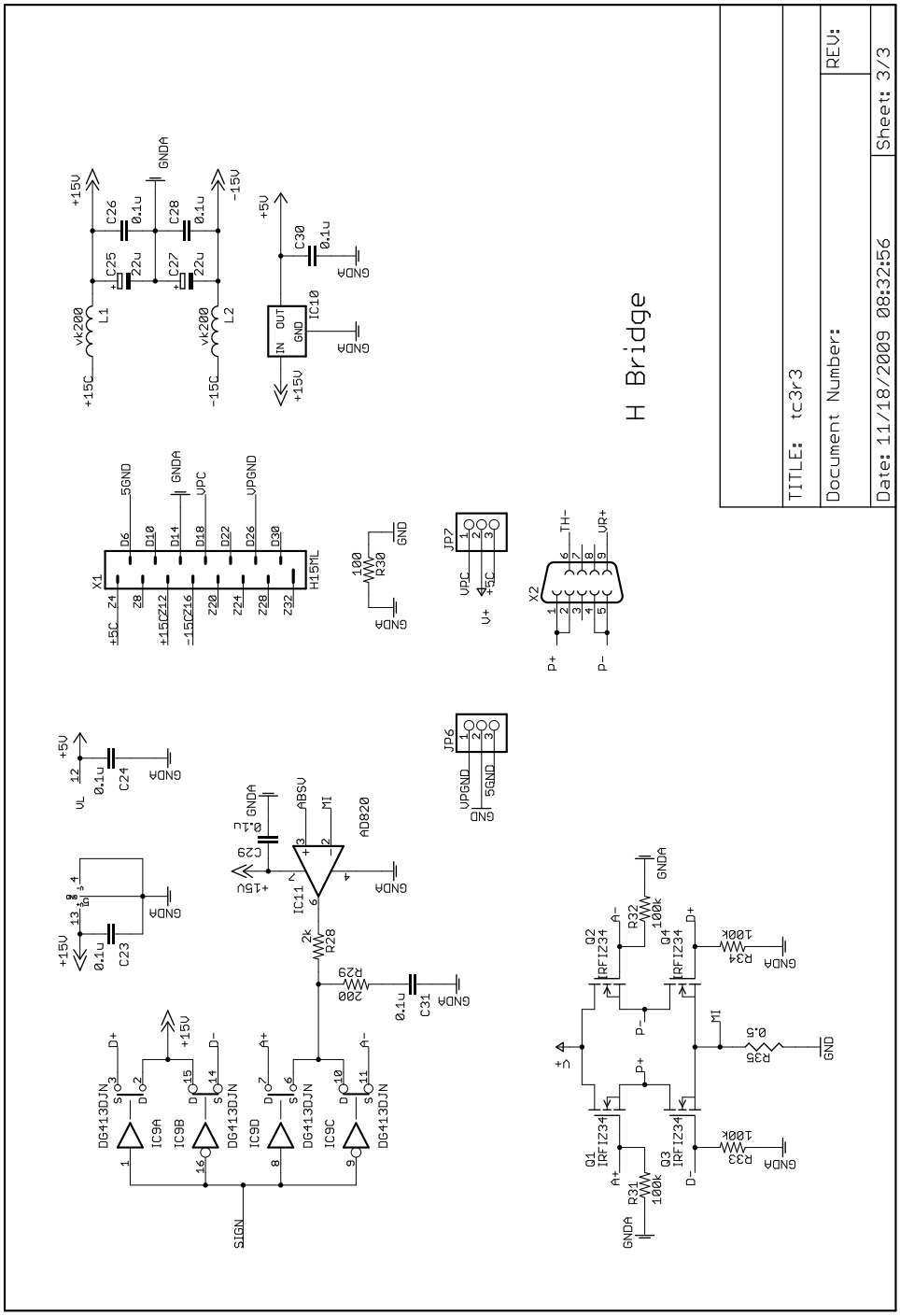

Figure 4: H bridge, supply, connectors.

The heat sink can be made using a 10mm thick, 70 mm long aluminium bar. With respect to the center of the bar two M3 threaded holes at ±28mm are used to fix the heat sink to the PCB. Two 3.1 mm holes at ±14mm can be used to fix Q1–4. An M3 threaded hole at 0 is required for R40.

Working at different temperatures

For modifying the working temperature few steps are required. As an example let's set the working temperature around $40C^\circ$ for heating a Rb cell, keeping the same tuning range of $40 \pm 5C^\circ$.

- Compute the new required value of R2 using Eq.(1) i.e. 5.35kΩ.
- Adjust the gain of IC1 to have again a sensitivity of $250\text{mV}/C^\circ$. In the example the new gain must be $9 \times 12.5/5.35 = 21$.
- Keep in mind that since the responsivity before IC1 has changed also the sensitivity to the external temperature has changed. In this case has increased by a factor $12.4/5.35 \sim 2.3$.

Heat only

In case a heating only circuit is needed just omit Q2, Q3 and IC9. Short pin 2,3 and pin 6,7 of IC9.

VCCS

For a VCCS the list of components to omit is longer so just have a look at Fig. 5, a silkscreen where only the required components have a visible part number. Use an insulated BNC to connect the input to JP2. IC4 will provide a differential input. Change the values of R13 and R21 to 10kΩ, replace C12 with a short and short JP4. In this way IC5B is a unity gain inverting amplifier. Adjust R18 for the desired sensitivity. Reducing C31 for higher bandwidth is a very bad idea unless you power supply likes short circuits. Some details in the next paragraph.

Bandwidth limit

When the bridge commutes it can potentially short the power supply. Suppose that Q1 and Q4 are on and Q2 and Q3 off. If the sign changes and the timing is wrong i.e. Q2 and Q3 turn–on before Q1 and Q4 switch–off the power supply is nearly shorted via R35. The turn–on time of Q3–4 is fairly fast and can be assumed negligible. The switch–off time is the discharge time of the gate capacitance (about 2nF for an IRFIZ34) via R33 or R34 so it is about 200μs.

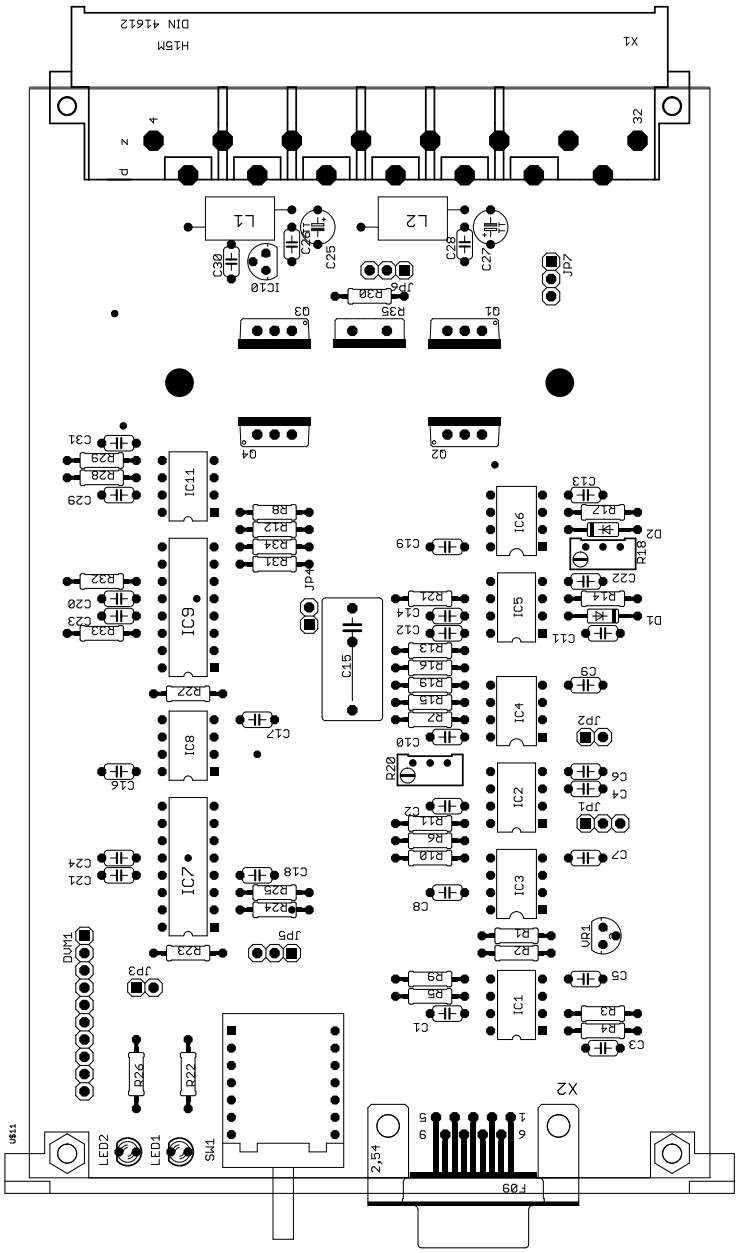

Figure 5: Silkscreen of the temperature controller.

The switch–off time of Q1–2 is roughly the same while the turn–on time is set by R28 and C31 again 200μs.

When commuting then Q3 will go immediately on shorting Q1 for about 200μs while Q4 will switch–off while Q2 turns–off roughly in the same time.

We are left only with the Q1–3 short. In a temperature controller this is not a problem because of the negligible slew–rate: the sign changes when Q1 is polarized for nearly zero current anyway. For a VCCS application it is necessary to limit the slew–rate at 0A to acceptable values i.e. something like 10mA/μs.

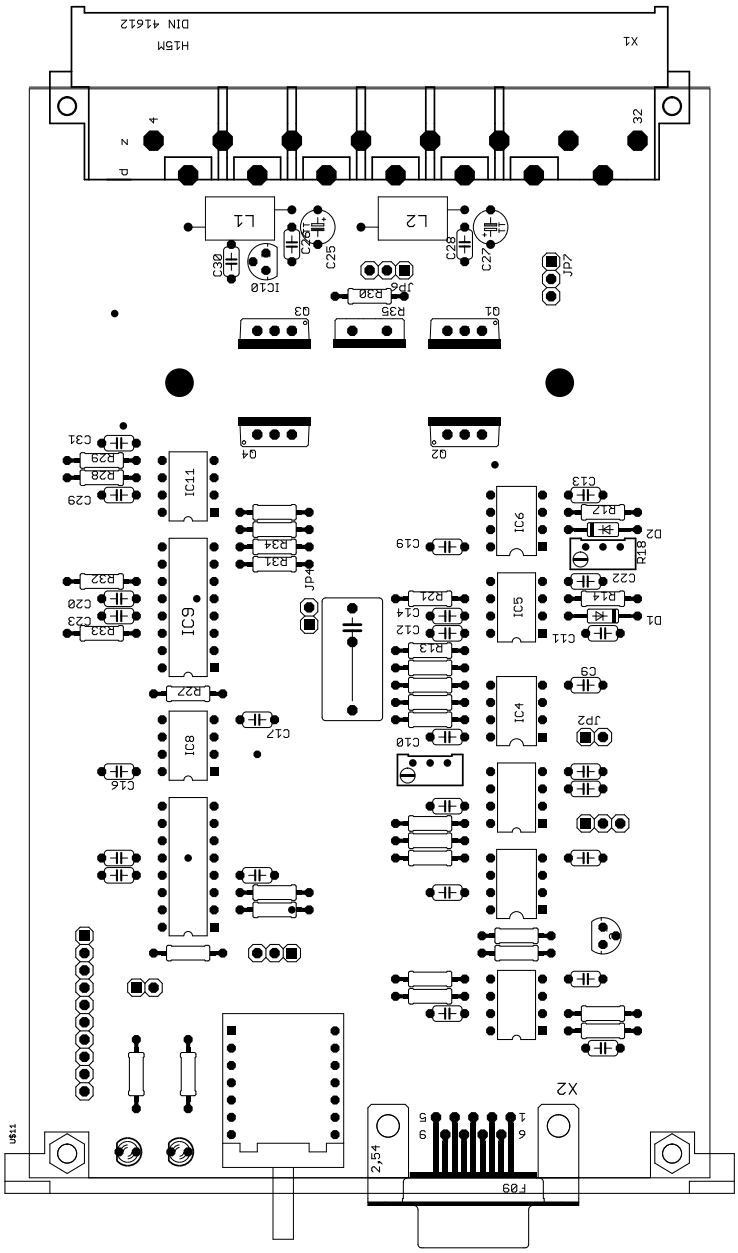

Figure 6: Silkscreen for a VCCS.